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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/596,720	06/22/2006	Samuel Anderson	681443-1U1	9904

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EXAMINER	
GUPTA, RAJ R	
ART UNIT	**PAPER NUMBER**
2814	

NOTIFICATION DATE	DELIVERY MODE
12/29/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/596,720	ANDERSON, SAMUEL	
	Examiner	Art Unit	
	RAJ GUPTA	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/13/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Attorney's Docket Number: 681443-1U1

Filing Date: 4/21/2006

371 Date: 6/22/2006

Claimed Domestic Priority: 4/22/2005 (US 60/673935)

Claimed Foreign Priority: NONE

Applicant: Anderson

Examiner: Raj R. Gupta

DETAILED ACTION

This Office Action responds to the amendment filed on 10/28/2009 and the IDS filed on 11/13/2009.

Acknowledgment

1. The amendment filed on 10/28/2009, responding to the Office Action mailed on 4/28/2009, has been entered. The present Office Action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office Action are **claims 1-26**.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1-26** are rejected under 35 U.S.C. 102(e) as being anticipated by **Hshieh et al (US 2006/0205174)**.

4. With regard to **claim 1**, Hshieh et al (US 2006/0205174, hereinafter Hshieh) teaches in Fig 23: A method of manufacturing a semiconductor device comprising: providing a semiconductor substrate having first (P- Epitaxial layer) and second main surfaces (P++ Substrate) opposite to each other, the semiconductor substrate having a heavily doped region of a first conductivity type (P++) at the second main surface and having a lightly doped region of the first conductivity type (P-) at the first main surface (501); providing in the semiconductor substrate a plurality of trenches (see Fig 2, 9 for exemplary trenches) and a plurality of mesas (see Fig 2, 11 for exemplary mesas) with each mesa having an adjoining trench (clearly visible in Fig 2) and a first extending portion extending from the first main surface toward the heavily doped region to a first depth position (clearly visible in Fig 2), at least one mesa having a first sidewall surface and a second sidewall surface, each of the plurality of trenches having a bottom (all of these structures clearly visible in Fig 2) (Fig 23, step 501); doping with a dopant of a second conductivity type the first sidewall surface of the at least one mesa to form a first doped region of the second conductivity type (504); doping with the dopant of the second conductivity type the second sidewall surface of the at least one mesa to form a second doped region of the second conductivity type (505); doping with a dopant of the first conductivity type the first sidewall surface of the at least one mesa to provide a second doped region of the first conductivity type at the first sidewall (507), and doping with the dopant of the first conductivity type the second sidewall surface of the at least one mesa to provide a fourth doped region of the first conductivity type at the second sidewall (508); lining at least the trenches adjacent to the at

least one mesa with an oxide material (513 and 503, also see Fig 27, 1506, and [0101]); and filling at least the trenches adjacent to the at least one mesa with one of a semi- insulating material and an insulating material (510).

5. With regard to **claim 2**, Hshieh teaches: the oxide lining is formed by one of low pressure (LP) chemical vapor deposition (CVD) Tetraethylorthosilicate (TEOS) and a spun- on-glass (SOG) deposition ([0075]).

6. With regard to **claim 3**, Hshieh teaches: forming a layer of undoped polysilicon, after the oxide lining step, over the trench bottoms and the mesas, each including the first and second sidewalls (Fig 23, 510).

7. With regard to **claim 4**, Hshieh teaches: the step of filling the plurality of trenches with one of a semi-insulating material and an insulating material includes filling the plurality of trenches with at least one of undoped polysilicon, doped polysilicon, doped oxide, undoped oxide, silicon nitride and semi-insulating polycrystalline silicon (SIPOS) (Fig 23, 510 and [0080]).

8. With regard to **claim 5**, Hshieh teaches: the first sidewall surface has a first predetermined inclination maintained relative to the first main surface and the second sidewall surface has a second predetermined inclination maintained relative to the first main surface ([0062]).

9. With regard to **claim 6**, Hshieh teaches: the first and second sidewall surfaces are generally perpendicular relative to the first main surface ([0063]).

10. With regard to **claim 7**, Hshieh teaches: the plurality of trenches are formed utilizing one or more of plasma etching, reactive ion etching (RIE), sputter etching, vapor phase etching and chemical etching ([0066]).

11. With regard to **claim 8**, Hshieh teaches: the implanting of the dopant of a second conductivity type into the first sidewall surface is performed at a first predetermined angle of implant (Fig 23, 504).

12. With regard to **claim 9**, Hshieh teaches: the doping with the dopant of a second conductivity type into the second sidewall surface is performed at a second predetermined angle of implant (Fig 23, 505).

13. With regard to **claim 10**, Hshieh teaches: the doping with the dopant of the first conductivity type into the first sidewall surface is performed at the first predetermined angle of implant (Fig 23, 507).

14. With regard to **claim 11**, Hshieh teaches: the doping with the dopant of the first conductivity type into the second sidewall surface is performed at the second predetermined angle of implant (Fig 23, 508).

15. With regard to **claim 12**, Hshieh teaches: diffusing the dopants of the second conductivity type into the at least one mesa prior to doping with the dopants of the first conductivity type (Fig 23, 506).

16. With regard to **claim 13**, Hshieh teaches: A semiconductor formed by the method of claim 1 (Fig 26, entire figure).

17. With regard to **claim 14** Hshieh teaches in Fig 20: A method of manufacturing a semiconductor device comprising: providing a semiconductor substrate having first (N- Epitaxial

layer) and second (N++ Substrate) main surfaces opposite to each other, the semiconductor substrate having a heavily doped region of a first conductivity type (N++) at the second main surface and having a lightly doped region of the first conductivity type (N-) at the first main surface (401); providing in the semiconductor substrate a plurality of trenches (see Fig 2, 9 for exemplary trenches) and a plurality of mesas (see Fig 2, 11 for exemplary mesas), with each mesa having an adjoining trench (clearly visible in Fig 2) and a first extending portion extending from the first main surface toward the heavily doped region to a first depth position (clearly visible in Fig 2), at least one mesa having a first sidewall surface and a second sidewall surface, each of the plurality of trenches having a bottom (all of these structures clearly visible in Fig 2) (Fig 20, step 401); doping with a dopant of the first conductivity type the first sidewall surface of the at least one mesa to form a first doped region of the first conductivity type (404); doping with a dopant of the first conductivity type the second sidewall surface of the at least one mesa to form a second doped region of the first conductivity type (405); doping with a dopant of the second conductivity type the first sidewall surface of the at least one mesa to provide a second doped region of the first conductivity type at the first sidewall (407), doping with the dopant of the second conductivity type the second sidewall of the at least one mesa (408); lining at least the trenches adjacent to the at least one mesa with an oxide material (412 and 403, also see Fig 28, 706); and filling at least the trenches adjacent to the at least one mesa with one of a semi-insulating material and an insulating material (410).

18. With regard to **claim 15**, Hshieh teaches: the oxide lining is formed by one of low pressure (LP) chemical vapor deposition (CVD) Tetraethylorthosilicate (TEOS) and a spun- on-glass (SOG) deposition ([0075]).

19. With regard to **claim 16**, Hshieh teaches: forming a layer of undoped polysilicon, after the oxide lining step, over the trench bottoms and the mesas, each including the first and second sidewalls (Fig 20, 410).

20. With regard to **claim 17**, Hshieh teaches: the step of filling the plurality of trenches with one of a semi-insulating material and an insulating material includes filling the plurality of trenches with at least one of undoped polysilicon, doped polysilicon, doped oxide, undoped oxide, silicon nitride and semi-insulating polycrystalline silicon (SIPOS) (Fig 20, 410 and [0080]).

21. With regard to **claim 18**, Hshieh teaches: the first sidewall surface has a first predetermined inclination maintained relative to the first main surface and the second sidewall surface has a second predetermined inclination maintained relative to the first main surface ([0062]).

22. With regard to **claim 19**, Hshieh teaches: the first and second sidewall surfaces are generally perpendicular relative to the first main surface ([0063]).

23. With regard to **claim 20**, Hshieh teaches: the plurality of trenches are formed utilizing one or more of plasma etching, reactive ion etching (RIE), sputter etching, vapor phase etching and chemical etching ([0066]).

24. With regard to **claim 21**, Hshieh teaches: the doping with the dopant of a second conductivity type of the first sidewall surface is performed at a first predetermined angle of implant (Fig 20, 404).

25. With regard to **claim 22**, Hshieh teaches: the doping with the dopant of a second conductivity type of the second sidewall surface is performed at a second predetermined angle of implant (Fig 20, 405).

26. With regard to **claim 23**, Hshieh teaches: the doping with the dopant of the first conductivity type of the first sidewall surface is performed at the first predetermined angle of implant (Fig 20, 407).

27. With regard to **claim 24**, Hshieh teaches: the doping with the dopant of the first conductivity type of the second sidewall surface is performed at the second predetermined angle of implant (Fig 20, 408).

28. With regard to **claim 25**, Hshieh teaches: diffusing the implanted dopants of the second conductivity type into the at least one mesa prior to implanting the dopants of the first conductivity type (Fig 20, 406).

29. With regard to **claim 26**, Hshieh teaches: A semiconductor formed by the method of claim 14 (Fig 24, entire figure).

Response to Arguments

30. Applicant's arguments filed 10/28/2009 have been fully considered but they are not persuasive.

31. The Applicants argue:

> Hshieh fails to disclose lining the trenches adjacent to the mesa with an oxide material after doping of the sidewalls and prior to filling the trenches.

32. The Examiner responds:

33. This is not a claimed limitation. Hshieh teaches lining at least the trenches adjacent to the at least one mesa with an oxide material in Fig 23, items 513 and 503; Fig 27, item 1506; and paragraph [0101], as is claimed in claims 1 and 14.

Conclusion

34. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

35. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to RAJ GUPTA whose telephone number is (571)270-5707. The examiner can normally be reached on Monday-Thursday 9am-6pm.

37. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571)272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

38. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

RAJ GUPTA
Examiner, Art Unit 2814
December 17, 2009

/Howard Weiss/
Primary Examiner
Art Unit 2814